

Our Ref.: 925-222  
534570

# ***U.S. PATENT APPLICATION***

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***Invention:*** SEMICONDUCTOR DEVICE AND PROCESS FOR MANUFACTURING THE  
SAME

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## ***SPECIFICATION***

## SEMICONDUCTOR DEVICE AND PROCESS FOR MANUFACTURING THE SAME

## BACKGROUND OF THE INVENTION

Field of the Invention

5           The present invention provides a capacitor for a ferroelectric memory and the like, and a process for manufacturing the same. More particularly, the present invention relates to a process for manufacturing a semiconductor device which has a capacitor comprising a lower electrode layer, a ferroelectric layer and an upper electric layer, which can suppress a peeling between the layers while maintaining electrical properties of the ferroelectric layer.

Prior Art

15           Recently, a ferroelectric memory has focused attention in a semiconductor field. A ferroelectric memory is a memory in the next generation which is characterized by a quick response, a random access, multiple rewriting, a low consumption power and the like. In the current ferroelectric memory, a transistor is formed, followed by formation of a capacitor comprising an electrode and a ferroelectric layer. These steps are usual processes as described in the Example of JP-A 11-214655. An embodiment of the prior art will be explained using Figures 5 and 6 below.

25           First, on an underlying substrate 21 on which a transistor

has been formed, an adhesion layer 22 is deposited to 50 nm by sputtering, for example,  $\text{TiO}_2$ ,  $\text{TiN}$  and the like. A lower electrode layer 23 is deposited thereon to 200 nm by sputtering, for example,  $\text{Pt}$ ,  $\text{Ir}$ ,  $\text{IrO}_3$  and the like. In addition, for example, SBT, PZT and the like is deposited by a Sol-Gel method, MOD, LSMC, sputtering, CVD and the like to 200 nm to form a ferroelectric layer 24 thereon, and which is sintered in an  $\text{O}_2$  atmosphere. Further, an upper electrode layer 25 is deposited thereon to 100 nm by sputtering, for example,  $\text{Pt}$ ,  $\text{Ir}$ ,  $\text{IrO}_3$  and the like (Figure 5A).

After that, a 1.5- $\mu\text{m}$  thick photoresist pattern 26 for processing the upper electrode is formed on the upper electrode layer 25 and, then, the upper electrode 25 is processed by dry etching (Figure 5B). Dry etching is performed mainly by sputter etching with Ar by highly dissociating a mixture gas of  $\text{Cl}_2$  and Ar under a high vacuum at 3 mTorr or less, for example, on a high density plasma etching apparatus using an Inductive Coupling Plasma (ICP) and the like. Generally, since vapor pressures of Pt and Ir are very low due to their low reactivity, Pt and Ir dissociated by sputter etching re-adhere to a sidewall of the pattern even after etching. By adding  $\text{Cl}_2$ ,  $\text{F}_2$  and the like to the etching gas, materials adhering on the sidewall are converted to chlorine or fluorine and the like so that they can be removed in the later step of washing.

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Then, an etching depot 27 adhering to the sidewall of the

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pattern is removed and, subsequently, a remaining resist pattern is removed by using a down flow  $O_2$  ashing apparatus and the like (Figure 5C).

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Subsequently, a 2.0- $\mu m$  thick photoresist pattern 28 for processing a ferroelectric layer is formed on the processed upper electrode layer 25 and the ferroelectric layer 24, and the ferroelectric layer 24 is processed by dry etching (Figure 5D). Since a ferroelectric layer has similar etching properties to those of Pt, Ir and the like, etching is performed under similar conditions and by a similar mechanism to those for etching the upper electrode layer.

After that, the etching depot 29 adhering to the pattern side wall is removed by washing and, then, a remaining resist is removed by down flow  $O_2$  ashing and the like (Figure 6E).

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Sub B6  
Similarly, a 2.0- $\mu m$  thick photoresist pattern 30 for processing a ferroelectric layer is formed on the processed upper electrode layer 25, the processed ferroelectric layer 24 and the lower electrode layer 23, and the lower electrode layer 23 is processed by dry etching (Figure 6F).

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Since the lower electrode layer is made from a similar material to that for the upper electrode layer, etching is performed by using a similar condition and mechanism.

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After that, the etching depot 31 adhering to the pattern side wall is removed by washing and, then, a remaining resist is removed by down flow  $O_2$  ashing and the like (Figure

Sub  
B7 end 6G).

When the capacitor shape is formed according to the above steps, the ferroelectric properties are deteriorated by dry etching and washing. Therefore, at the last step, after  
5 processing the capacitor, the ferroelectric layer is re-sintered by annealing at a temperature as high as or higher than the carcing (or sintering) temperature at which the ferroelectric layer is formed, to recover its electrical properties. By undergoing the above steps, the capacitor of the ferroelectric  
10 layer is formed.

However, this conventional process has a problem that a layer-peeling phenomenon occurs between an electrode layer and a ferroelectric layer when a capacitor is formed.

The layer-peeling phenomenon occurs when a depot is washed after etching each of the layers, and in a final annealing. Therefore, it can be considered that a lift-off phenomenon caused by penetration of a solution for washing a depot into a gap between the electrode layer and the ferroelectric layer, and interlayer separation due to a difference in a layer shrinkage rate between  
15 the electrode layer and the ferroelectric layer in annealing  
20 directly result in the layer peeling.

From an examination of the conventional semiconductor devices, it is demonstrated that peeling of the upper electrode layer tends not to occur as the surface morphology of the  
25 ferroelectric layer is worse, and that as the better surface

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morphology of the ferroelectric layer, that is, the denser film density results in the better electric properties. Therefore, it is currently difficult to accomplish to improve electrical properties and to decrease film peeling simultaneously, resulting in a big problem.

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SUMMARY OF THE INVENTION

10 Against the above problem, although a method is proposed for preventing the peeling by putting a dielectric layer with a high adherability between the electrode layer and the ferroelectric layer, it has disadvantages such as deterioration in electrical properties of the ferroelectric layer, process complication and the like and, therefore, an optimal method has not been established yet.

15 Thus, an object of the present invention is to suppress the peeling phenomenon in a semiconductor device comprising at least a ferroelectric layer and an upper electrode formed thereon while maintaining the electrical properties of the ferroelectric layer.

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20 According to the present invention, since a convex or concave region is formed on a surface of a first layer by etching, peeling between the first layer on which the convex or concave region has been formed and an upper layer formed on the first layer, which is caused by penetration of a bath or a layer shrinkage in a step of heating, is prevented (referred to as  
25

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encl

an "anchor effect").

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#### BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view illustrating a semiconductor device of an embodiment according to the present invention.

Sub B13  
Figure 2 is a cross-sectional view illustrating a step of manufacturing a semiconductor device of an embodiment according to the present invention.

Sub B14  
10 Figure 3 is a cross-sectional view illustrating a step of manufacturing a semiconductor device of an embodiment according to the present invention.

Sub B15  
15 Figure 4 is a cross-sectional view illustrating a step of manufacturing a semiconductor device of an embodiment according to the present invention.

Sub B16  
Figure 5 is a cross-sectional view illustrating a step of manufacturing a semiconductor device according to a conventional technique.

20 Figure 6 is a cross-sectional view illustrating a step of manufacturing a semiconductor device according to a conventional technique.

Sub B17  
Figure 7 is a schematic illustration showing film peeling which occurs in a conventional semiconductor device.

Detailed process will be explained below.

First, a problem of peeling between an upper electrode and a ferroelectric layer beneath the upper electrode layer is explained. After a ferroelectric layer is formed, a resist pattern is formed on a region in which the upper electrode is processed and formed. The ferroelectric layer is, then, etched to make a convex pattern on the surface of the ferroelectric layer. The size of this pattern should be controlled so that the convex pattern does not lap over outside of the upper electrode pattern in the subsequent step of forming the upper electrode with considering fluctuation in a pattern line width, an alignment deviation and the like. That is, a line width of the resist pattern for making the convex pattern is made to be narrower than the minimal line width of the upper electrode by a margin for the alignment deviation.

An etching depth of the ferroelectric layer is adjusted to the thickness of the upper electrode or smaller, since when the etching depth is larger than the thickness of the upper electrode, the upper electrode cannot be sputtered successfully, and the etching depth of the ferroelectric layer is adjusted to half of the thickness of the upper electrode or larger in order to exhibit the anchor effect. Further, from the viewpoint of the electrical properties of the ferroelectric layer, it is required that the etching depth of the ferroelectric layer is adjusted to half of its thickness or smaller.



Sub B19  
5 After etching the ferroelectric layer, a depot and the remaining resist layer are removed by washing and ashing and, then, an upper electrode is formed by sputtering. By carrying out subsequent processes after the formation of the upper electrode, peeling can be prevented due to the anchor effect as compared with the case where the upper electrode attaches a smooth ferroelectric layer. The above-mentioned means can be applied to an interface between the lower electrode and the ferroelectric layer to obtain the anchor effect.

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#### Example

The present invention will be explained in detail based on the following Examples.

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15 A semiconductor device according to the Example of the present invention is shown in Figure 1. As shown in Figure 1, the semiconductor device of the present invention is characterized in that an upper electrode 17 and a ferroelectric layer 14 have a convex region. By this constitution, a layer peeling can be suppressed. In this Example, one convex region is formed on one layer, but a plurality of convex regions may be formed on one layer. Alternatively, a concave region may be  
20 formed in place of the convex region.

Sub B21  
25 Figures 2A ~ D, Figures 3E ~ H, and Figures 4I ~ K are schematic illustrations showing procedures for manufacturing the semiconductor device shown in Figure 1.

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0.1  $\mu\text{m}$  and that for the alignment shift is 0.2  $\mu\text{m}$ , the specification for the resist pattern size is then within 0.7  $\mu\text{m}$ .

Subsequently, the resist pattern 15 is used as a mask to etch the ferroelectric layer 14 (Figure 2C). As etching conditions, for example, a high density plasma ICP etcher is used and the settings are as follows: Source power 2000 W; Bias power 500 W; Pressure 3 mTorr;  $\text{Cl}_2/\text{Ar}$  flow rate 30/90 sccm; and Etching depth 50 nm or greater and below 100 nm.

Sub B23  
10 After etching, an etching depot 16 adhering to the pattern sidewall is removed by washing (e.g., by dipping into 10% concentration hydrochloric acid for 30 seconds) and, then, the remaining resist pattern 15 is removed by ashing (e.g., on a microwave down flow ashing apparatus: Microwave power 1000 W; Wafer temperature 250 °C;  $\text{O}_2$  flow rate 1000 sccm; Treatment time 3 minutes) (Figure 2D).

Sub B24  
An upper electrode layer 17 is formed on the ferroelectric layer 14 thus fabricated by depositing, for example, Pt, Ir,  $\text{IrO}_3$ , and the like at a thickness of 100 nm by a conventional method such as sputtering (Figure 3E).

Sub B25  
20 Next, a photoresist is applied on the upper electrode 17 at a thickness of 1.5  $\mu\text{m}$  by spin-coating. Then, a photoreticle for fabricating the upper electrode is used to expose and develop the photoresist in order to form a resist pattern 18. Subsequently, the resist pattern 18 is used as a mask to etch the upper electrode layer 17 (Figure 3F). As etching conditions,

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Sub B25 end  
5 for example, a high density plasma ICP etcher is used and the settings are as follows: Source power 2000 W; Bias power 500 W; Pressure 3 mTorr;  $\text{Cl}_2/\text{Ar}$  flow rate 30/90 sccm; and Etching depth 115 nm (15% overetching based on the thickness of the upper electrode with considering a thickness fluctuation 10% and a etching rate fluctuation 10%).

Sub B26  
10 After etching, an etching depot 19 adhering to the pattern sidewall is removed by washing (e.g., by dipping into 10% concentration hydrochloric acid for 30 seconds) and, then, the remaining resist pattern 18 is removed by ashing (e.g., on a microwave down flow ashing apparatus: Microwave power 1000 W; Wafer temperature 250 °C;  $\text{O}_2$  flow rate 1000 sccm; Treatment time 3 minutes) (Figure 3G).

Sub B27  
15 Next, a photoresist is applied at a thickness of 1.5  $\mu\text{m}$  by spin-coating. Then, a reticle for fabricating the ferroelectric layer is used to expose and develop the photoresist in order to form a resist pattern 1a. Subsequently, the resist pattern 1a is used as a mask to etch the ferroelectric layer 14 (Figure 3H). As etching conditions, for example, a high density  
20 plasma ICP etcher is used and the settings are as follows: Source power 2000 W; Bias power 500 W; Pressure 3 mTorr;  $\text{Cl}_2/\text{Ar}$  flow rate 30/90 sccm; and Etching depth 115 % based on the thickness of the remaining ferroelectric layer.

Sub B28  
25 After etching, an etching depot 1b adhering to the pattern sidewall is removed by washing (e.g., by dipping into 10%

Sub B28 end  
 concentration hydrochloric acid 30 seconds) and, then, the remaining resist pattern 1a is removed by ashing (e.g., on a microwave down flow ashing apparatus: Microwave power 1000 W; Wafer temperature 250 °C; O<sub>2</sub> flow rate 1000 sccm; Treatment time 3 minutes) (Figure 4I).

Sub B29  
 10 Next, a photoresist is applied thereon at a thickness of 2.0 μm by spin-coating. Then, a photoretic for fabricating the lower electrode is used to expose and develop the photoresist in order to form a resist pattern 1c. Subsequently, the resist pattern 1c is used as a mask to etch the lower electrode layer 13 (Figure 4J). As etching conditions, for example, a high density plasma ICP etcher is used and the settings are as follows: Source power 2000 W; Bias power 500 W; Pressure 3 mTorr; Cl<sub>2</sub>/Ar flow rate 30/90 sccm; and Etching depth 230 nm (15% overetching based on the thickness of the upper electrode with considering a thickness fluctuation 10% and a etching rate fluctuation 10%).

Sub B30  
 20 After etching, an etching depot 1d adhering to the pattern sidewall is removed by washing (e.g., by dipping into 10% concentration hydrochloric acid 30 seconds) and, then, the remaining resist pattern 1c is removed by ashing (e.g., on a microwave down flow ashing apparatus: Microwave power 1000 W; Wafer temperature 250 °C; O<sub>2</sub> flow rate 1000 sccm; Treatment time 3 minutes) (Figure 4K).

Sub B31  
 25 Finally, in order to recover of the ferroelectric layer from a damage in the electrical properties caused by etching,

1. The first part of the document is a list of names and addresses, which appears to be a directory or a list of contacts. The names are written in a cursive script, and the addresses are listed below them. The list includes names such as "J. H. Smith", "W. J. Jones", and "A. B. Brown", among others. The addresses are also written in cursive and include street names and city names.

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